REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove. In response to the Office Action dated 07/12/2006, the Applicants submit this Amendment in order to prepare this case for appeal.

Claims 1-10 are pending and rejected. Claims 11-18 are withdrawn from consideration. Claims 1 and 10 are amended hereinabove.

Independent Claim 1 positively recites annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions. These advantageously claimed features are not taught or suggested by the patents of Bu et al. and Iwasaki; either alone or in combination.

Bu et al. does not teach the advantageously claimed invention because Bu et al. does not teach annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions (column 4 lines 12-18). Similarly, Iwasaki does not teach the advantageously claimed invention because Iwasaki does not teach annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions (column 8 lines 18-25). Rather, Iwasaki teaches away from the advantageously

claimed invention because Iwasaki teaches "cap annealing" that is "performed while a silicon dioxide film…is formed…" (column 8 lines 18-25). Therefore, the combination of Bu et al. and Iwasaki does not teach annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions, as advantageously claimed.

The Applicants respectfully traverse the statement on page 7 of the Office Action that "it would have been obvious to combine Iwasaki with Bu to obtain the invention as specified." The Applicants submit that those of ordinary skill in the art would not combine a method of fabricating GaAs MES FET transistors (Iwasaki) with a method for fabricating a CMOS transistor (Bu et al.) because the process parameters are mutually exclusive (e.g. materials used, precursors used, temperatures used, etc.).

Regarding the comments on page 2 of the Office Action, the Applicants respectfully traverse the statement that the "citation presented by the Applicant's representative is teaching the disadvantages of "capless" annealing." The Applicants submit that their citation of column 8 lines 18-25 refers to "cap annealing" (column 8 line 18), not capless annealing.

Regarding the comments on page 4 of the Office Action, the Applicants respectfully traverse the statement that "the methods of forming a oxynitride listed

in claim 6…" The Applicants submit that Claim 6 does not specify "oxynitride"; rather Claim 6 specifies "an interfacial layer of nitrogen". The Applicants note that the formation of "oxynitride" is taught by Bu et al. and involves the use of a silicon source gas (column 3 lines 43-47) during a (typically CVD) deposition process. Conversely, the advantageously claimed interfacial layer of nitrogen is incorporated into the existing structure at the specified location.

Due to the foregoing reasons, the Applicants respectfully traverse the Examiner's rejection of Claim 1 and respectfully assert that Claim 1 is patentable over Bu et al. and Iwasaki; either alone or in combination. Furthermore, Claims 2-9 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the references of record.

Independent Claim 10 positively recites annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions at a temperature in the range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds. These advantageously claimed features are not taught or suggested by the patents of Bu et al. and Iwasaki; either alone or in combination.

Bu et al. does not teach the advantageously claimed invention because Bu et al. does not teach annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions (column 4 lines 12-18). Similarly, Iwasaki does not teach the advantageously claimed invention because Iwasaki does not teach annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions (column 8 lines 18-25). Rather, Iwasaki teaches away from the advantageously claimed invention because Iwasaki teaches "cap annealing" that is "performed while a silicon dioxide film…is formed…" (column 8 lines 18-25). Therefore, the combination of Bu et al. and Iwasaki does not teach annealing, after the formation of the capping layer and with the capping layer in place, the extension and source and drain regions, as advantageously claimed.

The Applicants respectfully traverse the statement on page 7 of the Office Action that "it would have been obvious to combine Iwasaki with Bu to obtain the invention as specified." The Applicants submit that those of ordinary skill in the art would not combine a method of fabricating GaAs MES FET transistors (Iwasaki) with a method for fabricating a CMOS transistor (Bu et al.) because the process parameters are mutually exclusive (e.g. materials used, precursors used, temperatures used, etc.).

Due to the foregoing reasons, the Applicants respectfully traverse the Examiner's rejection of Claim 10 and respectfully assert that Claim 10 is patentable over Bu et al. and Iwasaki; either alone or in combination.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,

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